**Implementation of *Dadda Algorithm* and its applications**

**Abstract**

Multiplication algorithms have considerable effect on processors performance.A new high speed, low-power multiplication algorithm has been presented using modified Dadda tree structure.Two important modifications have been implemented in a partial product generation and reduction stage. In this paper, we proposed a new algorithm to reduce power, delay, and transistor count of a multiplication algorithm using Two’s complement negation rules. This work presents a novel design for Dadda multiplication algorithms. The proposed multiplication algorithm has achieved 44 per cent improvement in transistor count, 90 per cent reduction in delay and 89.9 per cent improvement in power consumption in compared with conventional designs. The modified version greatly reduces power required and number of adders.

**Tools:**

* Modelsim 6.4b
* Xilinx 10.1

**Languages:**

* VHDL/Verilog HDL